
LIST OF REFERENCES CITED BY APPLICANT
(Use several sheets if necessary)

ATTY. DOCKET NO.:

85170-4800

APPLICATION SERIAL NO.:

10/679,978

APPLICANT:

Stephen Maxwell PARKES

FILING DATE:

October 6, 2003

GROUP:

2819

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*


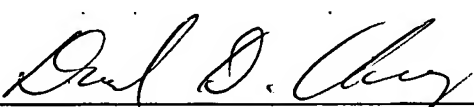
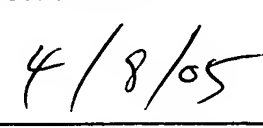
DC	AA	Guerrier et al. "A Generic Architecture for On-Chip Packet-Switched Interconnections", Proceedings of the Design Automation and Test in Europe, pages 250-256, Paris, France, March 2000.
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EXAMINER

DATE CONSIDERED

4/8/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AA							
	AB							
	AC							
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							YES NO	
<i>OK</i>	AD	JP 060118141	6/1985	Japan	—	—		X
<i>OK</i>	AE	JP 4151854 (English abstract)	5/1992	Japan	—	—	X	
<i>OK</i>	AF	JP 010255347 (English abstract)	9/1998	Japan	—	—	X	
<i>OK</i>	AG	WO 95/04404	2/1995	PCT	—	—	X	
<i>OK</i>	AH	WO 02/058355	7/2002	PCT	—	—	X	
	AI							
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AJ							
	AK							
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DC	AA	Search Report for Patents concerning "Object Oriented IC Architecture", NERAC, Inc., February 27, 2001, 21 pages					
DC	AB	Search Report for Patents concerning "On-Chip Packet Switching Networks, Etc.", NERAC, Inc., February 27, 2001, 61 pages					
DC	AC	"IEEE Heterogeneous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction)", IEEE Computer Society, September 21, 1995, 144 pages					
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